1   **HIGH-SPEED COMMUNICATION SYSTEM**

2   **WITH A FEEDBACK SYNCHRONIZATION LOOP**

3

4   Para Segaram

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6   <u>CROSS-REFERENCE TO RELATED APPLICATION</u>

7   This application is a continuation-in-part of application serial no. 09/372,319,

8   filed August 11, 1999. The entirety of application serial no. 09/372,319 as originally

9   filed including its originally-filed claims is incorporated herein by reference.

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11   <u>FIELD OF THE INVENTION</u>

12   The present invention relates to a high-speed communication system and, more

13   particularly, to a high-speed communication system with a feedback synchronization

14   loop.

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16   <u>DESCRIPTION OF THE RELATED ART</u>

17   A gigabit communication system is a system that transfers billions of bits of data

18   per second between the nodes of the system. Gigabit communication systems commonly

19   handle the data transferred over the backplane of the internet, and are expected to handle

20   the data transferred between next-generation processors and peripherals, such as hard

21   drives and printers.

22   FIG. 1 shows a block diagram that illustrates a conventional gigabit

23   communication system 100. As shown in FIG. 1, system 100 includes a high-speed

24   transmission medium 108, such as a fiber optic cable, and a number of communication

25   devices 110 that receives data from, and transmits data to, medium 108.

26   Each communication device 110, in turn, includes a physical layer device 112 that

27   is connected to medium 108, and a processing device 114 that is connected to physical

28   layer device 112 by a number of lines 116. Physical layer device 112 includes a

29   serializer/deserializer (serdes) that transforms data received from medium 108 into a

1 signal format that is compatible with processing device 114, and transforms data from

2 processing device 114 into a signal format that is compatible with medium 108.

3 When transferring data to, and receiving data from, processing circuit 114, the

4 serdes typically utilizes a data signal which has a logic high that is represented by a

5 maximum voltage which is equal to the supply voltage used by the processing circuit.

6 For example, when device 114 is formed in a 0.35 micron photolithographic

7 process, physical layer device 112 transmits data to, and receives data from, device 114

8 with data signals that have a maximum voltage of approximately 3.3V, the supply voltage

9 commonly used with 0.35 micron devices.

10 One channel of data is typically transported across medium 108, and between

11 physical layer device 112 and processing device 114, at 1.25 Gb/s, with speeds of 2.5

12 Gb/s under consideration. Processing device 114 processes the data received from

13 medium 108 by physical layer device 112, and outputs processed data to physical layer

14 device 112 for transmission onto medium 108.

15 Physical layer device 112 and processing device 114 are typically encapsulated in

16 separate chips which are placed on the same printed circuit board due to the largely

17 analog nature of device 112 and the largely digital nature of device 114. One

18 consequence of this approach, however, is that electromagnetic interference (EMI)

19 requirements limit the maximum speed that data can be exchanged between devices 112

20 and 114.

21 For example, when data is exchanged between devices 112 and 114 with data

22 signals having a maximum voltage of approximately 3.3V, the maximum speed that can

23 be obtained without exceeding the EMI requirements is approximately 125 Mb/s.

24 Thus, to handle one channel of inbound data, which is received at 1.25 Gb/s, 10

25 inbound lines 116 are required to transport data from device 112 to device 114, where

26 physical layer device 112 has 10 output ports and processing device 114 has 10 input

27 ports. (10 inbound lines 116 at 125 Mb/s provide one channel of inbound data at 1.25

28 Gb/s).

29 Similarly, processing device 114 requires 10 outbound lines 116 to transport one

30 channel of outbound data from device 114 to device 112, where processing device 114

1   has 10 output ports and physical layer device 112 has 10 input ports. Thus, device 112

2   and 114 each require 20 input/output ports, with 20 corresponding pins, to handle the

3   inbound and outbound data for one channel.

4   To provide additional EMI margin and greater chip-to-chip spacing,

5   communication devices with reduced chip-to-chip speeds are also available. These

6   reduced-speed devices typically transfer data between devices 112 and 114 at 62.5 Mb/s.

7   One problem with communication devices that have reduced chip-to-chip speeds,

8   however, is that devices 112 and 114 have twice as many I/O ports and twice as many

9   pins. Thus, with a reduced-speed device, devices 112 and 114 require 40 pins each (20

10   inbound lines 116 at 62.5 Mb/s are required to provide one input channel at 1.25 Gb/s,

11   while 20 outbound lines 116 at 62.5 Mb/s are required to provide one outbound channel

12   at 1.25 Gb/s).

13   The pin problem becomes even worse when devices 112 and 114 are packaged as

14   four- and eight-channel devices. When packaged in this way, devices 112 and 114, when

15   operating at a high chip-to-chip speed, i.e., 125 Mb/s, each require 80 pins and 160 pins

16   to support four- and eight-channel devices, respectively. Further, devices 112 and 114,

17   when operating at a slower chip-to-chip speed, i.e., 62.5 Mb/s, each require 160 pins and

18   320 pins to support four- and eight-channel devices, respectively.

19   The pin problem reaches critical stages when devices 112 and 114 are scaled up to

20   handle a 2.5 Gb/s data rate from the current 1.25 Gb/s rate. At these higher speeds,

21   devices 112 and 114, when operating at a high chip-to-chip speed, i.e., 125 Mb/s, require

22   160 pins and 320 pins to support four- and eight-channel devices, respectively. Further,

23   devices 112 and 114, when operating at a slower chip-to-chip speed, i.e., 62.5 Mb/s,

24   require 320 pins and 640 pins to support four- and eight-channel devices, respectively.

25   Thus, there is a great need to reduce the pin counts of devices 112 and 114 when

26   devices 112 and 114 are scaled up to handle a 2.5 Gb/s data rate. (In addition to

27   consuming huge amounts of silicon real estate, large pin count devices also consume

28   large amounts of power.)

29   One conceptual approach to reducing the pin counts is to exchange data between

30   devices 112 and 114 with a single-ended signal that has a lower maximum voltage. For

1   example, by lowering the maximum voltage of a single-ended data signal from 3.3V to

2   500 mV, the frequency of the data signal can be increased from 125 Mb/s to

3   approximately 1.25 Gb/s without exceeding the EMI requirements. By lowering the

4   maximum voltage from 3.3V to 250 mV, the frequency of the data signal can be

5   increased from 125 Mb/s to approximately 2.5 Gb/s without exceeding the EMI

6   requirements.

7   One problem with this conceptual approach, however, is that it is extremely

8   difficult, if not impossible, to form inbound detectors on processing device 114, and

9   outbound detectors on device 112, that accurately detect logic ones and logic zeros from

10 a single-ended gigahertz data signal that has a maximum voltage in the hundreds of

11 millivolts due to the voltage margins required by the detectors.

12   Another problem with this conceptual approach is that much more complex clock

13 recovery circuitry is required to recover a clock signal from a data signal operating in the

14 gigahertz range, such as 2.6 GHz, than from a data signal operating in the megahertz

15 range, such as 125 MHz. Thus, much of the clock recovery circuitry that is utilized in the

16 serdes would also be required in processing device 114 to recover the clock from a

17 gigahertz data signal (output by device 112 to device 114) that has a maximum voltage in

18 the hundreds of millivolts.

19   Another approach to reducing the pin count, that also avoids this duplication, is to

20 integrate the functions of physical layer device 112 and processing device 114 on a single

21 chip. One problem with this approach, however, is the incompatibility of high-precision

22 analog circuits, which make up most of the circuits on physical layer device 112, with

23 digital circuits, which make up most of the circuits on processing device 114.

24   One of these incompatibilities is the speed with which new processing

25 technologies can be implemented. For the present, digital circuits are easily adapted to

26 new (and smaller) processing technologies because the voltage levels that represent logic

27 ones in the new processing technologies are still easily distinguished from the voltage

28 levels that represent logic zeros.

29   For example, in both a 0.5 micron photolithographic process and a 0.35 micron

30 photolithographic process, where a logic one is represented by a 5V signal and a 3.3V

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1   signal, respectively, the logic one is easily distinguished from a logic zero which, in both

2   cases, has a voltage near zero.

3   For high-precision analog circuits, however, moving from a 0.5 micron

4   photolithographic process to a 0.35 micron photolithographic process, where the supply

5   voltage drops from 5V to 3.3V, dramatically reduces, among other things, the dynamic

6   ranges of the analog devices. Further design (and time) is then often needed to develop

7   devices which operate in these ranges.

8   Thus, integrating the functions of physical layer device 112 and processing device

9   114 on a signal chip increases the time required for the digital circuitry in the integrated

10   device to take advantage of the reduced size and power requirements provided by a new

11   photolithographic process.

12   As a result, there is a need for a communication device that has a physical layer

13   device and a processing device which operate in the gigahertz frequency range with

14   substantially fewer pins.

15

16   SUMMARY OF THE INVENTION

17   In a communication device having a physical layer device and a processing device

18   connected to the physical layer device, the pin counts of the physical layer device and the

19   processing device are substantially reduced when operating with gigahertz signals by

20   utilizing millivolt differential signals. In addition, a calibration feedback loop

21   synchronizes the data and clock signals on the processing device, thereby eliminating the

22   need for a gigahertz clock recovery circuit on the processing device. By eliminating the

23   gigahertz clock recovery circuit (involving high speed analog circuitry) from the

24   processing device and keeping the high speed analog circuitry on the physical layer

25   device, the processing device with the more easily scalable digital circuitry can be scaled

26   down to take advantage of smaller geometry processing technologies without having to

27   redesign the high speed analog circuitry on the physical layer device.

28   A communications device in accordance with the present invention includes a

29   physical layer device that has a media driver connectable to a transmission medium, a

30   media receiver connectable to the transmission medium, and a serializer/deserializer

1   (serdes) connected to the media driver and the media receiver. The physical layer device

2   also includes a master circuit that is connected to the serdes. The master circuit has a first

3   physical layer data driver that drives a millivolt differential signal, and a first physical

4   layer data receiver.

5   The communications device further includes a processing circuit that has an

6   internal circuit, and a slave circuit connected to the internal circuit and the master circuit.

7   The slave circuit has a first processing data receiver connected to the first physical layer

8   data driver. The first processing data receiver outputs a first signal in response to

9   receiving the signal output from the first physical layer data driver. In addition, the slave

10   circuit further includes a first processing data driver which is connected to the first

11   physical layer data receiver, and connectable to the first processing data receiver.

12   In addition, the master circuit further includes a clock driver which is connected

13   to the serdes and outputs a millivolt differential signal, and the slave circuit further

14   includes a clock receiver connected to the clock driver. The clock receiver outputs a

15   clock signal in response to a signal received from the clock driver.

16   Further, the first processing data driver is connectable to receive the clock signal

17   from the clock receiver or the first signal from the first processing data receiver. The first

18   physical layer data receiver receives the clock signal when the first processing data driver

19   is connected to receive the clock signal, and receives the first signal when the first

20   processing data driver is connected to receive the first signal.

21   The master circuit additionally includes an aligner that is connected to the first

22   physical layer data receiver. The aligner receives the clock signal when the first physical

23   layer data receiver receives the clock signal, and the first signal when the first physical

24   layer data receiver receives the first signal. The aligner has phase comparison circuitry

25   that compares the phase of the clock signal received by the aligner with the phase of the

26   first signal received by the aligner to determine a phase difference.

27   The master circuit further includes a phase delay circuit that is connected to the

28   aligner, the serdes, and the first physical layer data driver. The aligner passes a plurality

29   of signals to the phase delay circuit that indicates the phase difference. The phase delay

30   circuit delays the signal output from the first physical layer data driver so that the first

1   signal received by the aligner is substantially in phase with the clock signal received by

2   the aligner.

3   A better understanding of the features and advantages of the present invention

4   will be obtained by reference to the following detailed description and accompanying

5   drawings which set forth an illustrative embodiment in which the principles of the

6   invention are utilized.

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8   <u>BRIEF DESCRIPTION OF THE DRAWINGS</u>

9   FIG. 1 is a block diagram illustrating a conventional gigabit communication

10   system 100.

11   FIG. 2 is a block diagram illustrating a communication device 200 (a

12   communication system involving physical layer device 210 and processing circuit 25) in

13   accordance with the present invention.

14   FIG. 3 is a graph illustrating the frequency F of the signal transmitted between the

15   chips versus the distance D that separates the chips in accordance with the present

16   invention.

17   FIG. 4 is a block diagram of the logic circuit of FIG. 2 in accordance with a

18   particular embodiment of the present invention.

19   FIG. 5 is a simplified waveform diagram of an operation of the logic circuit of

20   FIG. 4 when no embedded command is being detected.

21   FIG. 6 is a simplified waveform diagram of an operation of the logic circuit of

22   FIG. 4 when an embedded command is being detected.

23   FIG. 7 is a flowchart that illustrates a method of operation of the logic circuit of

24   FIG. 4.

25   FIG. 8 is a block diagram of the receiver of FIG. 2 in accordance with a particular

26   embodiment of the present invention.

27   FIG. 9 is a circuit diagram of the filter of FIG. 8 in accordance with a particular

28   embodiment of the present invention.

1   FIG. 10 is a simplified waveform diagram illustrating a technique for sending an

2   embedded command using a clock signal in accordance with a particular embodiment of

3   the present invention.

4   FIG. 11 is a simplified waveform diagram illustrating another technique for

5   sending an embedded command using a clock signal in accordance with a particular

6   embodiment of the present invention.

7   FIG. 12 is a simplified circuit diagram of a differential driver for sending an

8   embedded in accordance with a particular embodiment of the present invention.

9

10   DETAILED DESCRIPTION

11   FIG. 2 shows a block diagram that illustrates a communication device 200 in

12   accordance with the present invention. As shown in FIG. 2, device 200 includes a

13   physical layer device 210 and a processing circuit 250 that is connected to device 210.

14   Device 210 receives information from, and transmits information to, a high-speed

15   transmission medium 212, such as a fiber optic cable, while circuit 250 receives

16   information from, and transmits information to, device 210. Device 200 is, in one

17   embodiment, disposed on a line card of a router. The line card has a backplane connector

18   for connecting to a backplane of the router. Processing circuit 250 communicates with

19   the rest of the router via this backplane connector. The high-speed transmission medium

20   211 is one of many fiber optic cables by which router is coupled to the Internet.

21   Device 210 includes a low-voltage, differential receiver 214 that outputs a pair of

22   differential data signals RXR+ and RXR- in response to receiving a pair of differential

23   signals RX+ and RX- from medium 212, and a low-voltage, differential driver 216 that

24   outputs a pair of differential data signals TX+ and TX- to medium 212 in response to

25   receiving a pair of differential data signals TXT+ and TXT-.

26   Data is preferably received from, and transmitted to, medium 212 at either 1.25

27   Gb/s, 1.6 Gb/s, or 3.125 Gb/s. (The present invention is not limited to these frequencies,

28   and may be used with other frequencies.)

1   Receiver 214 and driver 216 are preferably low-voltage PECL optical and short

2   copper receivers and drivers, respectively. (The present invention is not limited to these

3   drivers and receivers, and may be used with other drivers and receivers.)

4   In addition, device 210 also includes a gigabit serializer/deserializer (serdes) 220

5   that transforms the data signals RXR+ and RXR- into differential input data signals DIN+

6   and DIN-, and transforms an output data signal DOUT into the data signals TXT+ and

7   TXT-. A switch S switchably connects the input data signals DIN+ and DIN- to lines L1

8   and L2 in response to a first logic state of a calibration command CMD.

9   Serdes 220 also includes a phase-locked-loop circuit 222 that outputs a base clock

10   signal (not shown) having, for example, a frequency of 250 MHz, and a series of phase-

11   delayed clock signals PD1-PDn which each have an equal phase delay. For example,

12   each of five delayed clock signals can have a 72 degree phase shift (5*72=360).

13   Serdes 220 further includes a multiplier/switch circuit 224 that multiplies the

14   frequency of the base clock signal to output a pair of differential master clock signals

15   MCLK+ and MCLK-. The master clock signals MCLK+ and MCLK- are preferably

16   output at either 1.25 Gb/s, 1.6 Gb/s, 1.6 Gb/s, 2.5 Gb/s, or 3.125 Gb/s. (The present

17   invention is not limited to these frequencies, and may be used with other frequencies.)

18   In addition, circuit 224 also forms a pair of differential slave clock signals SLV+

19   and SLV- having the same frequency as the master clock signals MCLK+ and MCLK-.

20   Switch S switchably connects the slave clock signals SLV+ and SLV- to lines L1 and L2

21   in response to a second logic state of the calibration command CMD so that the slave

22   clock signals SLV+ and SLV- are output onto lines L1 and L2 instead of the data signals

23   DIN+ and DIN-. Switch S therefore multiplexes either the data signals (DIN+ and DIN-)

24   or the slave clock signals (SLV+ and SLV-) onto lines L1 and L2 depending on the value

25   of CMD.

26   Serdes 220 is preferably implemented to comply with the IEEE 802.3z Gigabit

27   Ethernet standard. (The present invention is not limited to the 802.3z Standard, and may

28   be used with other standards.)

29   Device 210 further includes a master circuit 226 that is connected to serdes 220.

30   Master circuit 226, in turn, includes a logic circuit 228 that outputs a pair of differential

1   delayable signals DD+ and DD- in response to the signals on lines L1 and L2, and a

2   series of select signals SEL1-SELs. Thus, when the input data signals DIN+ and DIN-

3   are on lines L1 and L2, the delayable signals DD+ and DD- represent the input data

4   signals DIN+ and DIN-; and when the slave clock signals SLV+ and SLV- are on lines

5   L1 and L2, the delayable signals DD+ and DD- represent the slave signals SLV+ and

6   SLV-.

7   Logic circuit 228 preferably provides a number of data paths that include a

8   reference data path and a number of additional data paths that incrementally delay and/or

9   advance the differential signals passing through circuit 228. The signals passing through

10   circuit 228, in turn, follow the data path selected by the select signals SEL1-SELs. (The

11   present invention is not limited to circuit 228, and may be used with other selectably

12   delayable circuits.)

13   In addition, circuit 226 further includes a millivolt differential driver 230 that

14   outputs (in response to the master clock signals MCLK+ and MCLK-) a pair of

15   differential transmit clock signals TX CLK+ and TX CLK- onto lines 280 and 281,

16   respectively. Circuit 226 also includes a millivolt differential driver 232 that outputs (in

17   response to the delayable signals DD+ and DD-) a pair of differential transmit signals TX

18   DATA+ and TX DATA- onto lines 282 and 283, respectively.

19   Thus, the transmit clock signals TX CLK+ and TX CLK- represent the master

20   clock signals MCLK+ and MCLK-. In addition, the transmit signals TX DATA+ and TX

21   DATA- represent the input data signals DIN+ and DIN- when the delayable signals DD+

22   and DD- represent the input data signals DIN+ and DIN-; and the slave clock signals

23   SLV+ and SLV- when the delayable signals DD+ and DD- represent the slave clock

24   signals SLV+ and SLV-.

25   Drivers 230 and 232 preferably output the transmit clock signals TX CLK+ and

26   TX CLK- and the transmit signals TX DATA+ and TX DATA- at either 1.25 Gb/s, 1.6

27   Gb/s, 2.5 Gb/s, or 3.125 Gb/s. (The present invention is not limited to these frequencies,

28   and may be used with other frequencies.) Thus, when the transmit signals TX DATA+

29   and TX DATA- represent the input data signals DIN+ and DIN-, data is output from

30   device 210 at the same data rate that device 210 receives data from medium 212.

1   In addition, the transmit clock signals TX CLK+ and TX CLK- and the transmit

2   signals TX DATA+ and TX DATA- are preferably defined by the TIA/EIA-644 Low

3   Voltage Differential Signal (LVDS) Standard (which defines a 250mV differential

4   signal). (The present invention is not limited to the LVDS Standard, and may be used

5   with other low-voltage standards.) One of the advantages of the present invention is that

6   by using millivolt differential signals, the EMI problem encountered by conventional

7   systems is effectively eliminated.

8   Circuit 226 additionally includes a millivolt differential data receiver 234 that

9   outputs a receive signal RD in response to receiving a pair of differential transmit signals

10   RX DATA+ and RX DATA-.   Differential transmit signals RX DATA+ and RX DATA-

11   are received from lines 284 and 285, respectively.

12   Further, circuit 226 also includes a phase interpolation and aligner circuit 236 that

13   outputs a series of finer delayed signals FD1-FDm, each having the same frequency and

14   an equal phase delay, in response to each phase delayed signal PD. For example, if phase

15   delayed signal PD1 represents a 0 degree phase shift, phase delayed signal PD2

16   represents a 72 degree phase shift, and phase delayed signal PD3 represents a 144 degree

17   phase shift, then 36 finer delayed signals each having a 2 degree phase shift are formed

18   for signal PD1, i.e., 0 degree, 2 degrees, 4 degrees, ... 70 degrees, while 36 finer delayed

19   signals each having a 2 degree phase shift are formed for signal PD2, i.e., 72 degrees, 74

20   degrees, 76 degrees, ... 142 degrees.

21   The resolution required by the system determines the number of finer delayed

22   signals FD1-FDm that are used. For example, to have a one degree resolution rather than

23   a two degree resolution, 72 finer delayed signals each having a one degree phase shift are

24   formed for each of the phase delayed signals PD1-PDn.

25   As described in greater detail below, circuit 236 also utilizes the finer delayed

26   signals FD1-FDm to compare the phase of a first received signal RD received at a first

27   time and the phase of a second received signal RD received at a later time, and outputs

28   the select signals SEL1-SELs in response to the comparison such that the select signals

29   SEL1-SELs define a difference between the phases of the signals.

1   Circuit 226 further includes a data recovery circuit 240 that outputs data signal

2   DOUT and a recovered clock signal RCLK in response to the received signal RD and the

3   finer delayed signals FD1-FDm.

4   As noted above and as further shown in FIG. 2, device 200 also includes

5   processing circuit 250. Circuit 250, in turn, includes a slave circuit 252 and an internal

6   circuit 254 that is connected to slave circuit 252. Slave circuit 252 includes a millivolt

7   differential receiver 256 that outputs a processing clock signal PCLK in response to

8   receiving the clock signals TX CLK+ and TX CLK-, and a millivolt differential receiver

9   258 that outputs a received signal RDATA in response to receiving the transmit signals

10   TX DATA+ and TX DATA-.

11   Thus, processing clock signal PCLK represents the master clock signal MCLK+

12   and MCLK-. In addition, the received signal RDATA represents the input data signals

13   DIN+ and DIN- when the transmit signals TX DATA+ and TX DATA- represent the

14   input data signals DIN+ and DIN-; and the slave clock signals SLV+ and SLV- when the

15   transmit signals TX DATA+ and TX DATA- represent the slave clock signals SLV+ and

16   SLV-.

17   Circuit 252 also includes a first shift register 260 that converts the serial received

18   signal RDATA into an input parallel data signal DATAIN in response to the processing

19   clock signal PCLK. Internal circuit 254 receives the processing clock signal PCLK and

20   the parallel data signal DATAIN.

21   The processing clock PCLK and the received signal RDATA have an equivalent

22   path length to the first shift register 260 (or a known phase delay). In addition, the

23   processing clock signal PCLK and the data signals DATAIN are CMOS (or otherwise)

24   compatible, and directly interface, with internal circuit 254.

25   In addition, circuit 252 further includes a second shift register 262 that directly

26   interfaces with internal circuit 254 to convert a parallel data signal DATAOUT from

27   internal circuit 254 into a serial data signal OUTD. Second shift register 262 utilizes the

28   processing clock signal PCLK to clock the parallel data signal DATAOUT out of shift

29   register 262. Thus the data signal OUTD is synchronized to the processing clock signal

30   PCLK.

1   Circuit 252 further includes a first multiplexor 264 that passes either the

2   processing clock signal PCLK or the received signal RDATA in response to a first mux

3   signal MUX1, and a second multiplexor 266 that passes either the processing clock signal

4   PCLK or the received signal RDATA, or the data signal OUTD in response to a second

5   mux signal MUX2. Further, the path lengths between receiver 256 and multiplexor 264,

6   and between receiver 258 and multiplexor 264 are equal (or have a known phase

7   difference).

8   In addition, circuit 252 includes a millivolt differential driver 270 that outputs the

9   differential transmit signals RX DATA+ and RX DATA- in response to either the

10   processing clock signal PCLK, the received signal RDATA, or the data signal OUTD,

11   depending on which signal is passed by multiplexor 266.

12   Circuit 252 further includes a logic circuit 272 that receives the processing clock

13   signal PCLK from shift register 262, and outputs mux signals MUX1 or MUX2 to

14   multiplexors 264 and 266 (or outputs a fixed pattern, e.g., 1-0-1-0-1-0, to shift register

15   262) in response to commands embedded in the processing clock signal PCLK (by serdes

16   220). Embedding commands in the processing clock is described in additional detail

17   below.

18   The transmit signals RX DATA+ and RX DATA- are preferably output at either

19   1.25 Gb/s, 1.6 Gb/s, 2.5 Gb/s, or 3.125 Gb/s. (The present invention is not limited to

20   these frequencies, and may be used with other frequencies.) Thus, the transmit signals

21   RX DATA+ and RX DATA- are output from circuit 250, received by device 210, and

22   output by device 210 to medium 212 at the same data rate.

23   In addition, the data signals RX DATA+ and RX DATA- are also preferably

24   defined by the TIA/EIA-644 Low Voltage Differential Signal (LVDS) Standard. (The

25   present invention is not limited to the LVDS Standard, and may be used with other low-

26   voltage differential signaling communication techniques.)

27   Thus, the received signal RD represents the data signal OUTD when the transmit

28   signals RX DATA+ and RX DATA- represent the data signal OUTD; the received signal

29   RDATA when the transmit signals RX DATA+ and RX DATA- represent the received

30   signal RDATA; and the processing clock signal PCLK, which represents the master clock

1   signal MCLK+ and MCLK-, when the transmit signals RX DATA+ and RX DATA-

2   represent the processing clock signal PCLK.

3   In addition, when the received signal RDATA represents the slave clock signals

4   SLV+ and SLV-, the received signal RD represents the slave clock signals SLV+ and

5   SLV-, and when the received signal RDATA represents the data signals DIN+ and DIN-,

6   the received signal RD represents the signals DIN+ and DIN-.

7   Device 210 and circuit 250 are formed in separate packages, and may be formed

8   on the same printed circuit board, or may be formed on separate circuit boards and

9   connected via a back plane or bus. In addition, the frequency of the signal transmitted

10 between the packages is a function of the distance that separates the packages.

11   FIG. 3 shows a graph that illustrates the frequency F of the signal transmitted

12 between the chips versus the distance D that separates the chips. As shown in FIG. 3, if

13 the chips are separated by 7.5cm, the maximum frequency F of the signal is

14 approximately 2.5 Gb/s; by 45cm, the maximum frequency F of the signal is

15 approximately 1.25 Gb/s; and by 5 meters, the maximum frequency F of the signal is

16 approximately 622 Mb/s. Thus, one of the advantages of the present invention is that

17 devices 112 and 114 can be further spaced apart, or placed on different circuit boards.

18   In operation, device 210 and circuit 250 include a calibration mode and a normal

19 operational mode. In the calibration mode, serdes 220 outputs the master clock signals

20 MCLK+ and MCLK- with an embedded command at the frequency of data RX+ and RX-

21 . In other words, the data and clock signals are at the same clock rate. As indicated

22 above and described in additional detail below, commands may be embedded in the

23 master clock signals.

24   The clock signals MCLK+ and MCLK- are driven by driver 230 as the clock

25 signals TX CLK+ and TX CLK-. In response to the clock signals TX CLK+ and TX

26 CLK-, receiver 256 outputs the processing clock signal PCLK to shift registers 260 and

27 262, and multiplexor 264.

28   The embedded clock command is passed through shift register 262 to logic circuit

29 272 which, in turn, sets the logic states of the MUX1 and MUX2 signals to pass the

30 processing clock signal PCLK through multiplexors 264 and 266. The processing clock

1   signal PCLK is then driven out of circuit 252 by driver 270 so that the transmit signals

2   RX DATA+ and RX DATA- represent the processing clock signal PCLK.

3   Receiver 234 outputs the received signal RD, which represents processing clock

4   signal PCLK, to aligner 236 in response to the transmit signals RX DATA+ and RX

5   DATA-. Aligner 236 compares the phase of the received signal RD with the finer

6   delayed signals FD1-FDm of each phase delayed signal PD, and identifies a finer delayed

7   signal FD that is closest in phase with the received signal RD. Thus, since the received

8   signal RD represents the processing clock signal PCLK which, in turn, represents the

9   master clock signals MCLK+ and MCLK-, aligner 236 identifies a finer delayed signal

10   FD that is closest in phase with the master clock signals MCLK+ and MCLK-.

11   In response to either a time out or a signal from aligner 236 that the phase of the

12   master clock signals MCLK+ and MCLK- has been identified, serdes 220 changes the

13   command embedded in the clock signals MCLK+ and MCLK-, and again outputs the

14   clock signals MCLK+ and MCLK-. In addition, serdes 220 also switchingly connects the

15   slave clock signals SLV+ and SLV- to lines L1 and L2.

16   The slave signals SLV+ and SLV- are passed through the reference data path and

17   output as the delayable signals DD+ and DD- which, in turn, are driven by driver 232 as

18   the transmit signals TX DATA+ and TX DATA-. In response to the transmit signals TX

19   DATA+ and TX DATA-, receiver 258 outputs the received signal RDATA, representing

20   the slave clock signals SLV+ and SLV-, which is presented to multiplexor 264.

21   As before, the clock signals MCLK+ and MCLK- are driven by driver 230 as the

22   clock signals TX CLK+ and TX CLK-. In response to the clock signals TX CLK+ and

23   TX CLK-, receiver 256 outputs the processing clock signal PCLK to shift registers 260

24   and 262, and multiplexor 264.

25   The embedded clock command is passed through shift register 262 to logic circuit

26   272 which, in turn, sets the logic states of the MUX1 and MUX2 signals to pass the

27   received signal RDATA through multiplexors 264 and 266. The received signal RD is

28   then driven out of circuit 252 by driver 270 as the transmit signals RX DATA+ and RX

29   DATA-.

1   Receiver 234 outputs the received signal RD, which represents the slave clock

2   signals SLV+ and SLV-, to aligner 236 in response to the transmit signals RX DATA+

3   and RX DATA-. Aligner 236 compares the phase of the received signal RD with the

4   finer delayed signals FD1-FDm of each phase delayed signals PD, and identifies a finer

5   delayed signal FD that is closest in phase with the received signal RD. Thus, since the

6   received signal RD represents the slave clock signals SLV+ and SLV-, aligner 236

7   identifies a finer delayed signal FD that is closest in phase with the slave clock signals

8   SLV+ and SLV-.

9   Aligner 236 compares the phase of the master clock signals MCLK+ and MCLK-

10   and the slave clock signals SLV+ and SLV-. Based on the comparison, the aligner 236

11   outputs select signals SEL1-SELs which identify a synch data path from the additional

12   data paths through logic circuit 228 such that, when the slave clock signals SLV+ and

13   SLV- on lines L1 and L2 pass through the synch data path, the phase of the master clock

14   signals MCLK+ and MCLK- and the phase of the slave clock signals SLV+ and SLV- are

15   in phase when arriving at aligner 236. (The present invention is not limited to aligner

16   236, and may be used with other circuits which determine the difference in phase

17   between the slave clock signals SLV+ and SLV- and the master clock signals MCLK+

18   and MCLK- to determine the appropriate select signals SEL1-SELs.)

19   Since the signal path for the signals that represent the master clock signals

20   MCLK+ and MCLK- and the slave clock signals SLV+ and SLV- is the same from

21   multiplexor 264 to aligner 236, the signals at the outputs of receivers 256 and 258 are

22   also synchronized. Further, the processing clock signal PCLK at the input to internal

23   circuit 254 and the parallel data signal DATAIN at the input to internal circuit 254 are

24   also synchronized as the skew associated with first shift register 260 is negligible.

25   As noted above, device 210 and circuit 250 also include a normal operational

26   mode. In the normal operational mode, multiplier/switch circuit 224 of serdes 220

27   outputs the clock signals MCLK+ and MCLK- with an embedded command at the

28   frequency of data RX, and switchably connects the data signals DIN+ and DIN- to lines

29   L1 and L2.

30   As a result, the received signal RDATA, which represents the input data signals

31   DIN+ and DIN-, is synchronously provided to first shift register 260 with the processing

16

1   clock signal PCLK. In addition, the embedded clock command is passed through shift

2   register 262 to logic circuit 272 which, in turn, sets the logic state of the MUX2 signal to

3   pass the data signal OUTD through multiplexor 266.

4   When working in the gigahertz range, simply providing equivalent path lengths

5   for the clock and data signals passing through device 210 and circuit 250, which are

6   formed in discrete packages, is insufficient to insure that the clock and data signals are

7   synchronized. This is because differences between the bonding leads and bonding

8   conductors of the discrete packages may unacceptably delay the clock signal with respect

9   to the data signal, or vice versa.

10   The present invention overcomes this problem by providing two independent

11   paths (for the clock and data signals) and one common feedback path. By synchronizing

12   the signals at the end of the common path (at aligner 236), the signals at the beginning of

13   the common path (at multiplexor 264) are also synchronized. By connecting the common

14   path to the independent paths in the package that supports circuit 250, the problems

15   caused by the differences between the bonding leads and bonding conductors of the

16   discrete packages are eliminated.

17   The present invention provides a number of advantages over the prior art. In

18   addition to eliminating the EMI problem as noted above, the present invention

19   significantly reduces the pin count of the packages that hold device 210 and circuit 250.

20   In the present invention, device 210 requires six pins for transmission and

21   reception with circuit 250, two each for drivers 230 and 232, and receiver 234. Similarly,

22   circuit 250 requires six pins for transmission and reception with device 210, two each for

23   receivers 256 and 258, and driver 270.

24   This compares with the 20 to 40 pins that are required per channel for each of the

25   prior art packages for transmission and reception between device 210 and circuit 250. By

26   substantially reducing the pin count, the present invention reduces the amount of silicon

27   real estate required to implement device 210 and circuit 250 which, in turn, reduces the

28   manufacturing costs and increases the manufacturing yield.

29   Another advantage is that, since device 210 and circuit 250 are formed in different

30   packages, devices 210 and circuit 250 can be formed with different processing

1 technologies. Digital circuit 250, including the analog elements in slave circuit 252, is

2 easily scaled down with advances in processing technology, e.g., 0.25 micron to 0.18

3 micron technologies, since there are so few analog devices in slave circuit 252. Device

4 210, which is largely analog and more difficult to scale down, can continue to use

5 existing processing technologies until newer processes have become proven.

6   A further advantage of the present invention is that by synchronizing the clock

7 and data signals on the slave circuit 252, the need for a clock recovery circuit on the slave

8 circuit 252 (to recover the clock from the data input from the physical layer device) is

9 eliminated. This saves additional silicon real estate and simplifies the design of the slave

10 circuit 252.

11   In accordance with an alternate embodiment of the present invention, a number of

12 channels, such as four or eight, can be utilized in lieu of a single channel. In the alternate

13 embodiment, each channel includes an inbound path having a line connected to serdes

14 220 and a logic circuit, a driver connected to the logic circuit, a receiver connectable to

15 the driver, and a shift register connected to the receiver. Each channel further includes an

16 outbound path having a shift register, a driver connectable to the shift register, a receiver

17 connectable to the driver and connected to data recovery circuit 240.

18   FIG. 4 is a more detailed view of an example embodiment of the logic circuit 272.

19 In this example, the logic circuit 272 includes a counter 300, an inverter 301 and a state

20 machine 302. The incoming PCLK signal from the receiver 256 is supplied to a clock

21 input lead 303 of the counter 300. The incoming PCLK signal is, in this example, a 2.5

22 GHZ clock signal.

23   The associated internal circuit 254 (as shown in FIG. 2) for this example includes

24 digital circuitry and a digital processor (i.e., a CPU) that may be clocked by a lower

25 frequency CPU CLK. The CPU CLK is supplied to an asynchronous clear input lead 304

26 of the counter 300. The CPU CLK is, in this example, a 300 MHz signal. The state

27 machine 302 is clocked by the CPU CLK received on a clock input lead 305. The state

28 machine 302 receives an embedded command detect signal on an input lead 306 and

29 outputs multiplexor (mux) select signals MUX1 and MUX2 on output leads 307 and 308, ·

30 respectively. The MUX1 signal is supplied to the select input lead of the multiplexor 264

31 as shown in FIG. 2 such that it controls which of the inputs of the multiplexor 264 is

1 passed to the multiplexor 266. The MUX2 signal is supplied to the select input lead of

2 the multiplexor 266 as shown in FIG. 2 such that it control which of the inputs (OUTD or

3 the signal received from multiplexor 264) is passed to the driver 270. Thus, these

4 multiplexor control signals determine if output data (OUTD) or one of the input signals

5 received by the receivers 256 and 258 is forwarded to the receiver 234 of the

6 communication device 200.

7 In normal operation, the clock signals TX CLK+ and TX CLK- on lines 280 and

8 281 are clocking at the 2.5 GHZ frequency. In order to put the processing circuit 250

9 into calibration mode, the physical layer device 210 sends an embedded command over

10 lines 280 and 281. The embedding of a command may be accomplished by stopping the

11 clocking of clock signals TX CLK+ and TX CLK- for a predetermined period of time.

12 The logic circuit 272 (or another embedded command detection circuit included in the

13 slave) detects this lack of clocking of PCLK as an embedded command.

14 In one example, a counter can be used in conjunction with the PCLK signal to

15 determine if enough pulses exist on the PCLK signal within a predetermined amount of

16 time. If a threshold number of pulses is not seen during the predetermined amount of

17 time, then it may be determined that an embedded command has been received. FIGs. 5

18 and 6 illustrate timing diagrams associated with example operations of such a system.

19 FIG. 5 illustrates the timing waveforms associated with normal operations where

20 an embedded command is not included in the PCLK signal. The bottom waveform, CPU

21 CLK, represents the clock supplied to the clear input lead 304 of the counter 300. The

22 counter 300 is held in a cleared state (outputs a four-bit value of 0000 for the specific

23 example provided) while the clock signal CPU CLK is high.

24 When the CPU CLK drops low at time T1, the counter 300 starts counting rising

25 edge transitions of PCLK. This counting is illustrated in FIG. 5 as a row of increasing

26 four-bit values labeled "COUNT". D0 is the least significant bit on counter 300 and

27 corresponds to the top most bit illustrated in this example. When the counter 300 counts

28 enough rising CPU CLK transitions such that the D2 bit of the counter 300 transitions

29 high (i.e. the counter 300 reaches the count value of four), then the counter 300 is

30 disabled via the active low count enable input lead 309 of the counter 300. This is

31 illustrated in FIG. 5 at time T2 where the count is halted at count 0100.

1   The inverter 301 inverts the value of bit D2 and supplies the resulting "embedded

2   command detect" signal to the input lead 306 of the state machine 302. During normal

3   operation (when an embedded command is not included in the PCLK signal), enough

4   pulses of the PCLK signal are received such that the threshold count is reached. As such,

5   the embedded command detect signal transitions low (i.e., no embedded command was

6   detected) before the state machine 302 clocks in the state of the "embedded command

7   detect" signal on the rising edge of CPU CLK at time T3.

8   FIG. 6 illustrates timing waveforms corresponding to a situation in which the

9   logic circuit 272 (or another embedded command detection circuit) detects that the PCLK

10 signal is not transitioning and, as a result, outputs an active high "embedded command

11 detect" signal. In the case of FIG. 6, although the counter 300 is enabled for counting

12 when CPU CLK transitions low at time T1, the counter 300 does not count any rising

13 edges of PLK. This is because the clock signals TX CLK+ and TX CLK- are kept from

14 toggling in order to communicate the embedded command. Accordingly, the counter

15 output bit D2 does not transition high and the embedded command detect signal remains

16 high. Based on the transition of CPU CLK at time T3, the state machine 300 reads in the

17 high state of the embedded command detect signal (i.e. an embedded command is

18 detected).

19 FIG. 7 includes a flow chart that illustrates an operation of the state machine 300.

20 The state machine 300 starts in a normal operation mode state (step 400). In the normal

21 operation mode, the multiplexor 266 supplies the data output from shift register 262 to

22 output driver 270 such that data is transmitted over lines 284 and 285 to physical layer

23 device 210. Accordingly, the multiplexor select signal MUX2 supplied to multiplexor

24 266 is driven such that the multiplexor 266 provides the data output OUTD to the input of

25 the driver 270. In the example illustrated in FIG. 7, a high value or logic "1" on the

26 MUX2 select signal is assumed to properly configure the multiplexor 266 to provide

27 OUTD at its output.

28 During normal operation, the signal selection performed by the multiplexor 264 is

29 inconsequential, as the output of the multiplexor 264 is not selected by the multiplexor

30 266. As such, the value driven on the control signal MUX1 is a "don't care", which is

31 represented by an "X" in FIG. 7.

1   At step 401, the state machine 302 determines if an embedded command has been

2   detected. In the example of FIG. 4, this is communicated to the state machine 302 on the

3   rising edge of the CPU CLK signal. As long as the clock signal PCLK is clocking at the

4   2.5 GHZ rate, an embedded command detect signal is not detected and the state machine

5   302 remains in the normal operation mode. This is illustrated in FIG. 7 by process flow

6   402. If the PCLK signal stops clocking for a predetermined period of time, the state

7   machine 302 detects an embedded command detect signal and proceeds to step 403.

8   At step 403, the master clock signal (MCLK+ and MCLK-) is selected as a

9   feedback signal to be provided back to the physical layer device 210. In the example

10   illustrated in FIG. 2, the master clock signal propagates across lines 280 and 281, through

11   the multiplexors 264 and 266, and back across lines 284 and 285. For simplicity of

12   discussion, this path is referred to as the master clock feedback path. For the example

13   illustrated, in order to configure the multiplexors to select the master clock signal as the

14   feedback signal, the multiplexor select signals MUX1 and MUX2 values are set to "1"

15   and "0" values, respectively. The phase of the master clock signal after transmission

16   along the feedback path is then measured within the physical layer device 210. Such

17   measurement may be referred to as calibration of the clock path as the lines 280 and 281

18   carry a clock signal during normal operation.

19   At step 404, the state machine 302 determines if another embedded command

20   detect signal is received. If not, the method returns (via process flow 405) to step 403

21   and the system remains configured to support the master clock feedback path. In one

22   embodiment, the subsequent embedded command detect signal is sourced by the physical

23   layer device 210 once the successful measurement of the phase of the master clock signal

24   received over the master clock feedback path is achieved.

25   If another embedded command detect signal is detected at step 404, the method

26   proceeds to step 406. At step 406, the multiplexors 264 and 266 are configured such that

27   the slave clock signal (made up of SLV+ and SLV-) is routed back to physical layer

28   device 210 as the feedback signal. In the example illustrated in FIG. 2, the slave clock

29   signal propagates across lines 282 and 283, through the multiplexors 264 and 266, and

30   back across lines 284 and 285. For simplicity of discussion, this path is referred to as the

31   slave clock feedback path.

1   For the example illustrated, in order to configure the multiplexors to select the

2   master clock signal as the feedback signal, the multiplexor select signals MUX1 and

3   MUX2 values are set to "0" and "0" values, respectively. The phase of the slave clock

4   signal after transmission along the slave clock feedback path is then measured within the

5   physical layer device 210 and compared with the phase of the master clock signal after

6   transmission along the master clock feedback path. Based on this comparison, the delay

7   of the logic block 228 is varied until the phase of the slave clock transmitted across the

8   slave clock feedback path has a desired phase relationship with the master clock signal as

9   transmitted across the master clock feedback path. In some embodiments, this may

10   require aligning the phases of the two signals, whereas in other embodiments a desired

11   phase offset (e.g. in degrees or time units) may be desired. This calibration operation may

12   be referred to as calibrating the data path as the lines 282 and 283 typically carry data

13   during normal operation.

14   Generally, the only difference between the master clock feedback path and the

15   slave clock feedback path is that the master clock feedback path includes lines 280 and

16   281 and their corresponding driver and receiver, while the slave clock feedback path

17   includes lines 282 and 283 and their corresponding driver and receiver. As such, the

18   phase calibration performed using the feedback paths can be used to establish a known

19   phase relationship for the signals transmitted across these components, thus allowing data

20   signals sent across lines 282 and 283 to be properly phase aligned with clock signals sent

21   across lines 280 and 281. This allows the data signals to be captured within the slave

22   circuit 252 without the need for complex clock recovery circuitry within the slave circuit

23   252.

24   Once the calibration of the data path is completed at step 406, another embedded

25   command may be used to return the state machine to normal operation at step 400. This

26   additional embedded command may be detected at step 407. If the additional embedded

27   command is not detected at step 407, the state machine returns to step 406 via process

28   flow 408.

29   In other embodiments, the transitions from step 403 to step 406 and from step 406

30   to step 400 may be controlled based on the expiration of a predetermined time delay

31   rather than receipt of additional embedded commands. For example, the state machine

1   may transition from normal operation to the clock path calibration step based on an

2   embedded command received and then transition to the calibrate data path state after a

3   predetermined time period during which the phase of the master clock signal is generally

4   assured of being measured. As is apparent to one of ordinary skill in the art, a longer

5   time period may be required to perform the data path calibration at step 406 such that the

6   time period spent at step 406 is greater than that spent at step 403.

7   FIG. 8 is a diagram of one example of a receiver 256 that includes circuitry for

8   detecting embedded commands that are communicated by an alteration of the common

9   mode voltage of a received differential signal. In such an embodiment, the clock signals

10 TX CLK+ and TX CLK- on input leads 500 and 501 have a common mode voltage

11 within a particular voltage range during normal operation. For example, in the case

12 where the voltage of each of signals TX CLK+ and TX CLK- ranges between VCC and

13 VCC minus 250 millivolts, the signals TX CLK+ and TX CLK- are controlled such that

14 the average voltage of TX CLK+ and TX CLK- over time (common mode voltage) is

15 within some specified range (for example, VCC minus 125 millivolts plus or minus ten

16 percent).

17   In order to communicate a command to the slave circuit 252, the physical layer

18 device 210 generates an embedded command using the signals on lines 280 and 281 by

19 shifting the common mode voltage outside the specified range. A state machine similar

20 to state machine 300 described above can be used in association with the receiver 256

21 depicted in FIG. 8. Such a state machine would utilize the embedded command detect

22 signal produced on output 505 to determine when to perform certain state transitions (and

23 other state transitions may be based on the expiration of a predetermined time period as

24 described above). The state machine 300 operates in accordance with the process flow of

25 FIG. 7 as described above, but rather than receiving and "embedded command detect"

26 signal from a counter such as counter 300, the "embedded command detect" signal is

27 received from receiver 256 of FIG. 8 (in this case via shift register 262).

28   The receiver 256 illustrated in FIG. 8 includes a first comparator 502 that utilizes

29 the differential signal received on input leads 500 and 501 to generate the clock signal

30 PCLK on output lead 503. As shown, the receiver 256 also includes a common mode

31 detect circuit 504 that generates the embedded command detect signal on lead 505.

1   The common mode detect circuit 504 detects when the common mode voltage

2   corresponding to the differential signal received over leads 500 and 501 exceeds a

3   specified voltage VREF. In a particular embodiment, VREF may be approximately VCC

4   minus 125 millivolts plus 12 millivolts. Thus, if the common mode voltage is raised 12

5   millivolts above its normal level, an embedded command is detected. As is apparent to

6   one of ordinary skill in the art, the value of VREF may be adjusted based on the

7   particular characteristics (voltage level, timing, etc.) of the differential signal over which

8   the embedded command is being carried.

9   The common mode detect circuit 504 includes a second comparator 506, a DC

10   filter (i.e., low pass filter) 507, and a voltage divider 508n that is used to generate VREF.

11   FIG. 9 is a circuit diagram of one example of a filter 507 that may be used to determine

12   the common mode voltage of the differential signal received over lines 500 and 501. As

13   is apparent to one of ordinary skill in the art, the polarity of the inputs to the comparator

14   506 may be reversed such that the embedded command is detected when the voltage on

15   the common mode voltage falls below a predetermined VREF threshold. In some

16   embodiments, the embedded command detect signal on lead 505 may be latched or edge

17   triggered to ensure that it is properly provided to the state machine that controls the

18   multiplexors 264 and 266.

19   FIG. 10 illustrates one technique that may be used by the physical layer device

20   210 to transmit an embedded command. In this case, the signals TX CLK+ and TX

21   CLK- that are carried over the lines 280 and 281 are held high for a period of time (T4)

22   sufficient for the receiver 256 to detect the elevated common mode voltage (designated

23   by a dashed line).

24   FIG. 11 illustrates another way that the physical layer device 210 may transmit an

25   embedded command. In this case, the voltage levels of each of the signals making up the

26   differential signal are increased by a predetermined shift voltage for a period of time (T5)

27   sufficient for receiver 256 to detect the reduced common mode voltage (designated by a

28   dashed line). The magnitude of the predetermined shift voltage is determined based on

29   the reference voltage VREF. The direction of the shift, which is upwards in the example

30   illustrated such that the common mode voltage is increased, may be determined by

31   whether the receiver 256 is configured to detect a common mode voltage that exceeds a

1   predetermined higher threshold level, falls below a predetermined lower threshold level,

2   or both.

3   FIG. 12 is a simplified diagram of a driver 230 that may be used in a system that

4   includes a receiver similar to that depicted in FIG. 8. In this circuit, additional current

5   sources 600 are turned on to increase the drop across the load resistors 601 and therefore

6   reduce the DC common mode voltage on the differential output signal 602. In other

7   cases, the current sources that are normally turned on may be turned off in order to

8   reduce the voltage drop across the load resistors and therefore increase the common mode

9   voltage on the differential output signal 602.

10   Although the embedded command is described being sent across the TX CLK+

11   and TX CLK- lines 280 and 281, it is to be understood that in other embodiments an

12   embedded command may be sent using the TX DATA+ and TX DATA- lines 282 and

13   283. In such embodiments, the receiver 258 would include the common mode voltage

14   deviation detection circuitry described with respect to FIGs. 8-11 above.

15   In one embodiment, both the driver 232 and the driver 230 have the structure of

16   FIG. 12. In such an embodiment, an embedded command may be communicated over

17   lines 280 and 281 for phase detection of the clock feedback path, whereas another

18   embedded command is communicated over lines 282 and 283 for phase

19   detection/calibration of the data feedback path. In order to detect the common mode shift

20   that signifies an embedded command, the receivers 256 and 258 may include analog

21   circuitry, such as that described with respect to FIG. 8 above, adapted for such common

22   mode shift detection.

23   Other techniques for conveying commands to the slave circuit 252 rely on the

24   particular data protocol utilized. For example, in normal operation, data may be

25   transmitted over lines 282 and 283 in accordance with one of many communication

26   protocols. In a Gigabit Ethernet 803.2z communication device, for example, data values

27   are converted into symbols that require additional bits of encoding. Such encoding

28   techniques are used for a variety of reasons, including prevention of base line wander,

29   simplification of receiver circuitry, etc. In one example, an eight-bit data value may be

30   encoded to produce a ten-bit symbol (8B/10B encoding) that is transmitted. Once

31   received, a 10B/8B decoder is used to convert the symbols back into the data values.

1   Only certain symbols are considered valid for the transmission of data values, and the

2   remaining symbols may be either unused or used for the communication of control

3   information.

4   In accordance with one embodiment of the present invention, the physical layer

5   device 210 transmits an embedded command to the processing circuit 250 by using a

6   predetermined encoded symbol or sequence of symbols. The decoder in the processing

7   circuit 250 can detect such symbols and indicate that an embedded command has been

8   detected. This can then be used to control a state machine similar to that illustrated in

9   FIG. 4. In other cases, different symbols or sequences represent different commands

10   corresponding to different desired results (i.e. one command configures the data feedback

11   path, another configures the clock feedback path, and another indicates normal

12   operation).

13   Although the physical layer device 210 controls the processing circuit 250 in the

14   examples above using an embedded command, it is to be understood that the command

15   need not be embedded. Thus, in some embodiments, one or more dedicated signal lines

16   or an additional communication signal or bus may be used to relay one or more different

17   commands to the processing circuit 250.

18   The phase-matching calibration process described above need not necessarily be

19   initiated by the physical layer device 210 sending a command to the processing circuit

20   250. For example, the processing circuit 250 may automatically enter the calibration

21   mode after power-up. The processing circuit 250 can switch the feedback path from the

22   clock feedback path to the data feedback path in response to receiving a command as

23   described above, or alternatively can automatically switch the feedback path after a

24   certain period of time.

25   In one embodiment, the calibration mode is entered in response to detecting a

26   particular condition. For example, if the processing circuit 250 detects a bit error rate

27   above a particular value (e.g., checksums associated with the data indicate a threshold

28   number of errors in the data transmission from the physical layer device 210 to

29   processing circuit 250), then the processing circuit 250 may signal the physical layer

30   device 210 of the need to perform a calibration. The physical layer device 210 then

1　　initiates and/or controls the phase calibration process described above such that the bit

2　　error rate is reduced to an acceptable level.

3　　　　　In another embodiment, the physical layer device 210 carries out the phase

4　　calibration process periodically in accordance with a predetermined schedule.

5　　Accordingly, the described phase calibration process may be executed in response to

6　　numerous different conditions and can be initiated and controlled in many different ways.

7　　Additionally, the signals passing between physical layer device 210 and processing

8　　circuit 250 may, in some embodiments, be single-ended signals rather than differential

9　　signals.

10　　　　　In the foregoing specification, the invention has been described with reference to

11　　specific embodiments. However, one of ordinary skill in the art appreciates that various

12　　modifications and changes can be made without departing from the scope of the present

13　　invention as set forth in the claims below. Accordingly, the specification and figures are

14　　to be regarded in an illustrative rather than a restrictive sense, and all such modifications

15　　are intended to be included within the scope of present invention.

16　　　　　Benefits, other advantages, and solutions to problems have been described above

17　　with regard to specific embodiments. However, the benefits, advantages, solutions to

18　　problems, and any element(s) that may cause any benefit, advantage, or solution to occur

19　　or become more pronounced are not to be construed as a critical, required, or essential

20　　feature or element of any or all the claims. As used herein, the terms "comprises,"

21　　"comprising," or any other variation thereof, are intended to cover a non-exclusive

22　　inclusion, such that a process, method, article, or apparatus that comprises a list of

23　　elements does not include only those elements but may include other elements not

24　　expressly listed or inherent to such process, method, article, or apparatus.

25